

--	--	--	--	--	--	--	--	--	--

**Third Semester B.E. Degree Examination, June/July 2016**  
**Logic Design**

Time: 3 hrs.

Max. Marks: 100

**Note: Answer any FIVE full questions, selecting  
 atleast TWO questions from each part.**

**PART - A**

- 1 a. Name universal gates. Realize basic gates using NAND gate only. (08 Marks)  
 b. Prove that symmetrical signal has a duty cycle of 50% and find the frequency, low and high duty cycles for asymmetrical signal if it is high for 3 ms and low for 4 ms. (08 Marks)  
 c. Explain the structure of VHDL/Verilog program. (04 Marks)
- 2 a. Find the SOP of the following Boolean function using K - map.  
 i)  $f(p q r s) = \Sigma m(6, 7, 9, 10, 11, 13) + d(0, 1, 8, 12)$   
 ii)  $f(a b c d) = \pi m(1, 2, 4, 9, 10, 12) + d(0, 3, 5)$ . (08 Marks)  
 b. Simplify  $f(A B C D) = \Sigma m(0, 1, 2, 3, 5, 8, 12, 14, 15)$  using Quine - McClusky method. (12 Marks)
- 3 a. Design a 16 : 1 multiplexer using two 8 : 1 multiplexers and one 2 : 1 multiplexers with expressions. (06 Marks)  
 b. With relevant diagram explain n-bit magnitude comparator. (08 Marks)  
 c. Give HDL implementation for 4 : 1 MUX using 'case' statement. (06 Marks)
- 4 a. What do you mean by characteristic equation of 'Flip-flop'? Draw the logic diagram, truth table and explain working of 'JK - Flip - Flop' and implement the same using NAND gate. (12 Marks)  
 b. With state table and state transition diagram, analyse the behaviour of sequential circuit shown in Fig. Q4(b). (08 Marks)

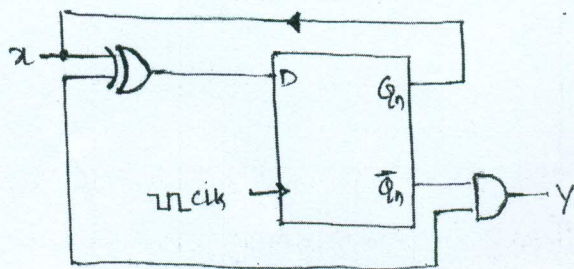


Fig. Q4(b)

**PART - B**

- 5 a. With a neat logic and timing diagram, explain the working of a 4 - bit SISO register. (10 Marks)  
 b. Design two 4 - bit number serial adder. (06 Marks)  
 c. Write verilog HDL code for 4 - bit SIPO shift register. (04 Marks)
- 6 a. Design synchronous modulus - 5 (mod -5) counter using JK - Flip-Flop. (10 Marks)  
 b. Explain, design of 4 - bit binary ripple - up counter using negative edge triggered JK - flip-flops with block diagram and timing diagram. (10 Marks)



- 7 a. With neat diagram explain and compare Mealy and Moore machine. (10 Marks)
- b. Reduce state transition diagram (Moore model) of Fig. Q7(b) by i) Row elimination method (10 Marks)  
ii) implication table method.

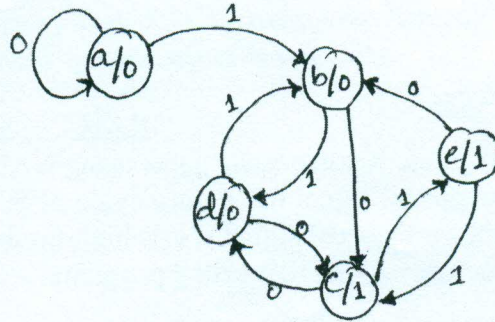


Fig. Q7(b)

- 8 a. Discuss the two drawbacks of resistive divider used in converting D/A. Draw the schematic for a 4-bit binary ladder and explain how the digital to analog conversion is achieved using it. (10 Marks)
- b. Discuss the working of following A/D converters : (10 Marks)
  - i) Successive approximation A/D
  - ii) Counter type A/D.

\*\*\*\*\*

Highly confidential document EDC - 104, © 20-11-2016 13:11:08